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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,188	03/01/2004	Reed A. Linde	42P15390	3180

8791 7590 05/04/2005

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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,188	LINDE ET AL.	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *March 1, 2004 through August 10, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-15,20,24-28 and 31* is/are rejected.

7)☒ Claim(s) *4,16-19,21-23,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *030104*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communications dated March 1, 2004 through August 10, 2004, claims 1-31 are active in this application.

Information Disclosure Statement

2. The information disclosure statement filed March 1, 2004 has been considered.

Claim Objections

3. Claims 4, 16-19, 21-23, 29, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the

purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-3 and 5-13 are rejected under 35 U.S.C 102(e) as being anticipated by Pekny [U.S. Patent #6,553,510].

With respect to claim 1, Pekny discloses a method comprising: detecting an electrical characteristic identifying a defect in a memory unit; and replacing the memory unit with an alternate memory unit, wherein the replacing is performed during user operation of a device having the memory unit and the alternate memory unit. See columns 1 and 2. In the cited columns, Pekny discloses that if particular memory is identified to be defective, it is replaced with alternate memory [redundant memory] during the erase and programming operation of the memory.

With respect to claims 2 and 3, Pekny discloses, in columns 1 and 2, that the detection of a defective memory is done during an erase and programming operation. Also see figures 4 and 5.

With respect to claim 5, Pekny discloses that the detection of a defective memory and replacement of the memory is done during an erase and programming operations. See columns 1 and 2 and also figures 4 and 5.

With respect to claim 6, Pekny discloses that once the defective memory is detected, its accessibility is routed to the replacement memory, thereby rendering the defective memory inaccessible.

With respect to claim 7, Pekny discloses, in column 5, lines 5-20, accessing the defected address will automatically route to the redundant memory.

With respect to claim 8, Pekny discloses a non-volatile memory with redundant memory structures. See columns 1 and 2.

With respect to claim 9, Pekny discloses that the memory contains programmable fuse. See columns 1 and 2.

With respect to claim 10, Pekny discloses the setting of addresses with regard to the redundant memory. See columns 1 and 2.

With respect to claim 11, Pekny discloses that the memory is a flash memory. See column 1.

With respect to claim 12, Pekny discloses that the memory is a flash memory. It is known that the memory is arranged in rows and columns. See column 1.

With respect to claim 13, Pekny discloses that he memory is a polymer. See column 1.

6. Claims 14 and 15 are rejected under 35 U.S.C 102(e) as being anticipated by Scheuerlein et al. [U.S. Patent #6,868,022].

With respect to claim 14, Scheuerlein et al. disclose, in figure 7, a plurality of accessible memory units [MEMORY ARRAY]; one or more redundant memory units [REDUNDANT ROWS – it has a plurality of sub-arrays]; a failure detection unit [700] coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and redundant block swap unit [770] coupled [indirectly] to the plurality of accessible

memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one of the one or more redundant memory units.

With respect to claim 15, Scheuerlein et al. disclose, in figure 7, that the failure detection circuit comprising: a current detection unit to detect a current during an erase operation.

7. Claim 20 is rejected under 35 U.S.C 102(e) as being anticipated by Santin [U.S. Patent #6,847,574].

With respect to claim 20, Santin discloses, in figures 1, 2 and 5, a processor [506]; an antenna [504] coupled to the processor [indirectly]; and a memory device [508] coupled to the processor, the memory device comprising: a plurality of accessible memory units [110]; one or more redundant memory units [108]; a failure detection unit [202] coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and a redundant block swap unit [206] coupled to the accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one or more redundant memory units.

8. Claims 24-28 are rejected under 35 U.S.C 102(e) as being anticipated by

Pekny [U.S. Patent #6,553,501].

With respect to claim 24, Pekny discloses an apparatus comprising: a computer readable medium [eeprom]; and instructions stored on the computer readable medium [see columns 1 and 2] to: detect an electrical characteristic that identifies a defect in a memory unit [302 of figure 3]; and replace the memory unit with an alternate memory unit [304 of figure 3], wherein replacing is performed during user operation of a device having the memory unit and the alternate memory unit. See columns 1 and 2. In the cited columns, Pekny discloses that if particular memory is identified to be defective, it is replaced with alternate memory [redundant memory] during the erase and programming operation of the memory.

With respect to claim 25, Pekny discloses that the detecting method includes monitor a current; and identify a defect when the current exceeds a predetermined current threshold. See columns 1-2 and figures 4 and 5.

With respect to claim 26, Pekny discloses that the detection method includes monitor a voltage during an erase attempt; and identify a defect when the voltage exceeds a predetermined voltage threshold. See columns 1-2 and figures 4 and 5.

With respect to claim 27, Pekny discloses that the detection of a defective memory is done by comparing its characteristics with references. See columns 1-2 and figures 4 and 5.

With respect to claim 28, Pekny discloses, in column 5, lines 5-20, accessing the defected address will automatically route to the redundant memory.

With respect to claim 31, Pekny discloses that the memory is a flash memory. See column 1.

Allowable Subject Matter

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- The failure detection circuit comprising: a voltage detection unit to detect a voltage during an erase operation.
- The failure detection circuit comprising: a resistance detection unit to detect a resistance during an erase operation.
- Wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
April 29, 2005

MICHAEL TRAN
PRIMARY EXAMINER